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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/590,251	08/17/2006	Eddie Huang	GB04 0044 US1	7154
65913	7590	02/17/2009	EXAMINER	
NXP, B.V.			NGUYEN, JOSEPH H	
NXP INTELLECTUAL PROPERTY DEPARTMENT			ART UNIT	PAPER NUMBER
M/S41-SJ			2815	
1109 MCKAY DRIVE				
SAN JOSE, CA 95131				
NOTIFICATION DATE		DELIVERY MODE		
02/17/2009		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/590,251	HUANG ET AL.	
	Examiner	Art Unit	
	JOSEPH NGUYEN	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 17 August 2006.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-8 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-8 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 17 August 2006 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>8/17/06</u> . | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Drawings

1. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 2-3 are objected to because of the following informalities: in claims 2-3, the term "each spaced region" should be corrected to read, "each said spaced region". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over figures 1-3 of the acknowledged prior art (APA) in view of Yokogawa et al. (U.S. Publication No. 2003/0227061).

Regarding claim 1, applicant admitted in figures 1-3 of (APA) it is well known in the art that a vertical trench gate semiconductor device comprising a semiconductor body 2 having a top major surface 2a and a plurality of trench gates comprising trenches 6 extending into the semiconductor body from the top surface with insulated gate electrode 4 therein, the semiconductor body comprising source and drain regions 8, 12 of a first conductivity type which are separated by a channel accommodating region 10 of a second, opposite conductivity type adjacent the trench gates wherein the trench gates extend in stripes (Fig. 1), the source regions extend transversely between the trench gates in stripes, projection of the source stripes across the trench gate defines intermediate trench portions between the projected source stripes. Also see page 2, lines 6-26 of the specification of the instant application. Figures 1-3 of (APA) do not show mutually spaced regions of the second conductivity type provided immediately below the intermediate trench portions which are connected to source potential. However, Yokogawa et al. discloses in figure 9(b) a vertical trench gate semiconductor device comprising mutually spaced regions 43 of the second conductivity type are provided immediately below the intermediate trench portions 51 which are connected to source potential 44 so as to increase the channel mobility (paragraphs [0101] and [0103]). In view of such teaching, it would have been obvious at the time of the present invention to modify figures 1-3 of (APA) by including mutually spaced regions of the

second conductivity type provided immediately below the intermediate trench portions being connected to source potential so as to increase the channel mobility.

Regarding claim 2, Yokogawa et al. discloses in figure 9(b) each spaced region 43 extends from the channel accommodating region 42.

Regarding claim 3, Yokogawa et al. discloses in figure 9(b) each spaced region 43 extends from the channel accommodating region 42 on one side of the trench 51 to meet the channel accommodating region on the other side of the trench.

Regarding claim 4, the combination of figures 1-3 of (APA) and Yokogawa et al. would disclose the depth of each trench oscillates along its length between depths above and below the lower boundary of the channel accommodating region such that the second conductivity type region (43 of Yokogawa et al.) that provides the channel accommodating region 42 extends periodically below the trench 51 to form the spaced regions.

Regarding claim 8, Yokogawa et al. discloses in figure 10(c) the method of manufacturing a vertical trench gate transistor semiconductor device of claim 1 having trenches 51 of substantially uniform depth comprising steps of forming a mask 51 over the top surface of the semiconductor body; and introducing dopant of the second conductivity type through the windows of the mask for the spaced regions 43 (paragraph [0108]).

5. Claims 1-2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over figures 1-3 of the acknowledged prior art (APA) in view of Hshieh et al. (U.S. Publication No. 2001/0003367).

Regarding claim 1, applicant admitted in figures 1-3 of (APA) it is well known in the art that a vertical trench gate semiconductor device comprising a semiconductor body 2 having a top major surface 2a and a plurality of trench gates comprising trenches 6 extending into the semiconductor body from the top surface with insulated gate electrode 4 therein, the semiconductor body comprising source and drain regions 8, 12 of a first conductivity type which are separated by a channel accommodating region 10 of a second, opposite conductivity type adjacent the trench gates wherein the trench gates extend in stripes (Fig. 1), the source regions extend transversely between the trench gates in stripes, projection of the source stripes across the trench gate defines intermediate trench portions between the projected source stripes. Also see page 2, lines 6-26 of the specification of the instant application. Figures 1-3 of (APA) do not show mutually spaced regions of the second conductivity type provided immediately below the intermediate trench portions which are connected to source potential. However, Hshieh et al. discloses in figure 2 a vertical trench gate semiconductor device comprising mutually spaced regions 130 of the second conductivity type are provided immediately below the intermediate trench portions 125 which are connected to source potential 140 so as to reduce the gate to drain interfacing areas and thus prevent the difficulty of slower switching speed caused by large gate to drain interfacing areas in a trench gate semiconductor device (paragraph [0014]). In view of such teaching, it would

have been obvious at the time of the present invention to modify figures 1-3 of (APA) by including mutually spaced regions of the second conductivity type provided immediately below the intermediate trench portions being connected to source potential so as to reduce the gate to drain interfacing areas and thus prevent the difficulty of slower switching speed caused by large gate to drain interfacing areas in a trench gate semiconductor device.

Regarding claim 2, Hshieh et al. discloses in figure 2 each spaced region 130 extends from the channel accommodating region.

Regarding claim 4, the combination of figures 1-3 of (APA) and Hshieh et al. would disclose the depth of each trench oscillates along its length between depths above and below the lower boundary of the channel accommodating region such that the second conductivity type region (130 of Yokogawa et al.) that provides the channel accommodating region extends periodically below the trench 51 to form the spaced regions.

6. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over figures 1-3 of (APA) and Yokogawa et al. or Hshieh et al. and further in view of Hsu et al. (U.S. Publication No. 2004/0145011).

Regarding claims 5-7, figures 1-3 of (APA) and Yokogawa et al. or Hshieh et al. together disclose all the structures set forth in claim 4 from which claims 5-7 depend. Since claim 4 is a product claim, claims 5-7 are reasonably treated as product claims herein. In this case, the language of claims 5-7 is merely product by process limitation.

MPEP § 2113 states that even though product by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend upon its method of production. If the product in the product by process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product made by a different process. *In re Thorpe*, 777, F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

On the other hand, if claims 5 and 7 are treated as a process claims, Hsu et al. disclose in figures 2A-2H all the steps of the method set forth in claims 5 and 7 (see pages 2-3). Note that the method used to form the device shown in figures 1-3 of (APA) would include the step of forming the trenches deeper than the lower boundary of the channel accommodating region and shallower than said lower boundary between source region stripes. In view of such teaching, it would have been obvious at the time of the present invention to further modify figures 1-3 of (APA) and Yokogawa et al. or Hshieh et al. by using the claimed method steps so as to effectively form an improved vertical trench gate semiconductor device.

Regarding claim 6, the Examiner takes the Official Notice that it only involves routine skill in the art to have the etchant etches the first mask material more slowly than the semiconductor body, since doing so would preserve the first mask on the top surface until the etching step of the semiconductor body is done such that there would be no undesired etched areas on the top surface of the semiconductor body.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 8:30 am- 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on (571) 272-2298. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kenneth A Parker/

Supervisory Patent Examiner, Art Unit 2815

/J. N./
Examiner, Art Unit 2815